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(54) Voltage controlled oscillator

(57) A voltage controlled oscillator with a substantially linear voltage/frequency characteristic employs in the resonant circuit of the oscillator, a variable capacitance (21 - 22 line only) related to the mutual conductance, g_{mv} of an associated amplifier and to a control voltage VS1 or current applied to the amplifier. Flow of RF current through terminal 22 may be avoided by using a balanced arrangement (Figs. 3A, 3B). In the figure, a variable capacitance is produced by the C, R, transistor combination and is linearly related to the voltage VS1.

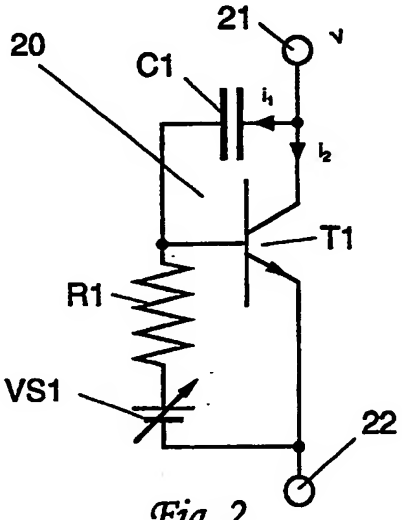

Fig. 2.

GB 2 288 502 A

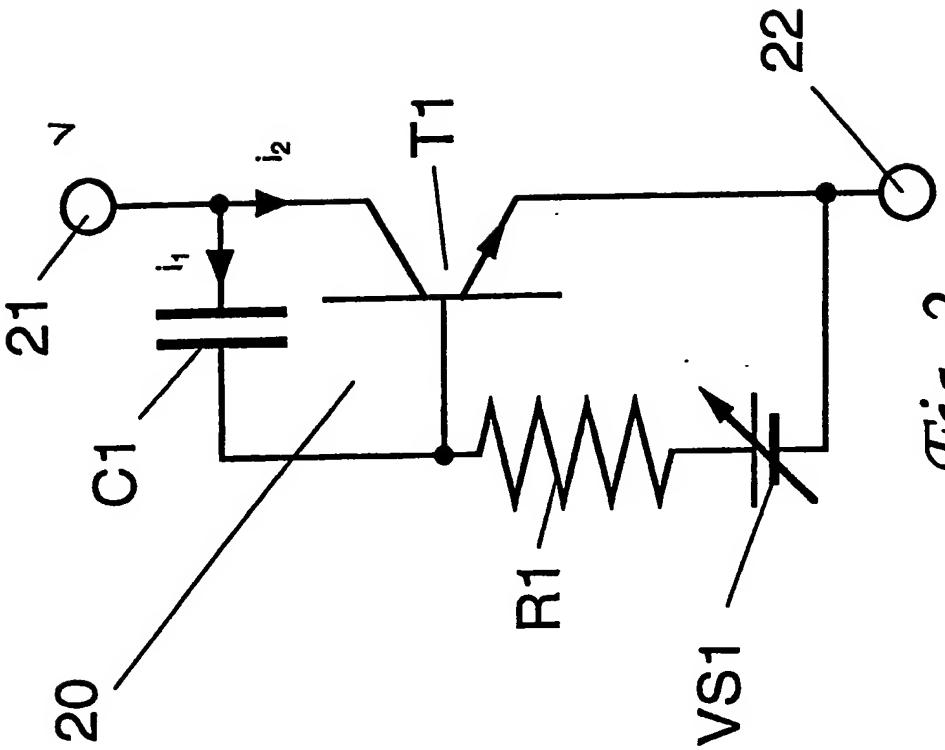

Fig. 2.

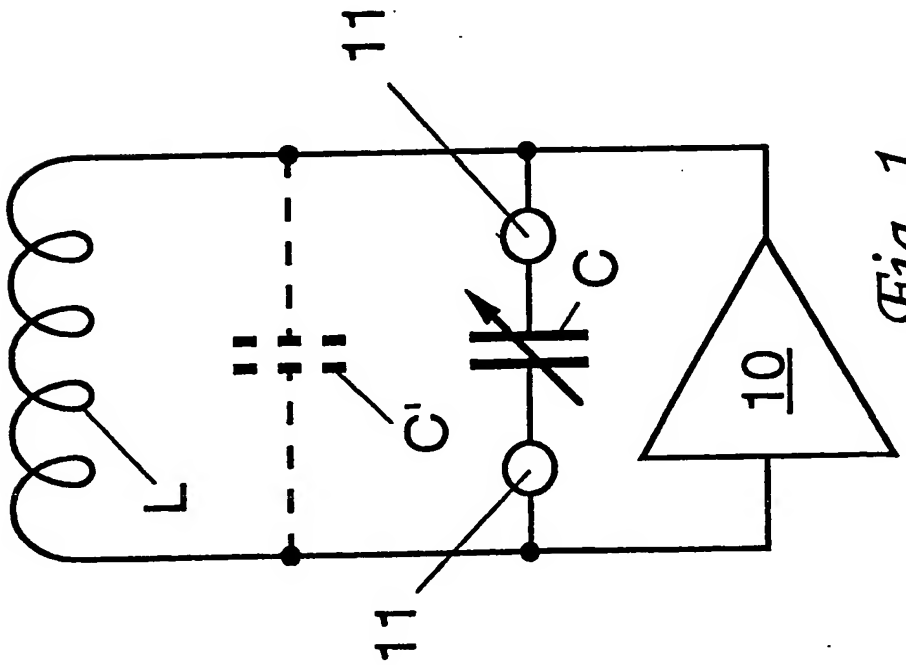

Fig. 1.

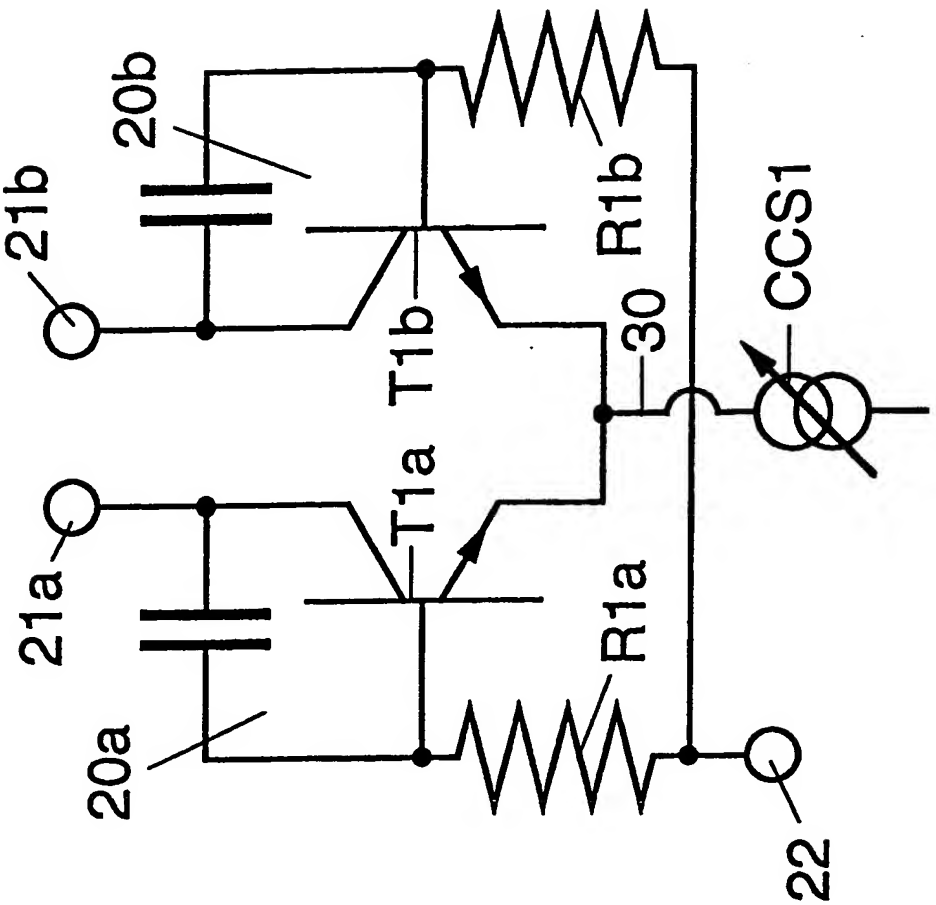
20b
21b
T1b
R1b
30
CCS1
21a
T1a
20a
R1a
22

Fig. 3B.

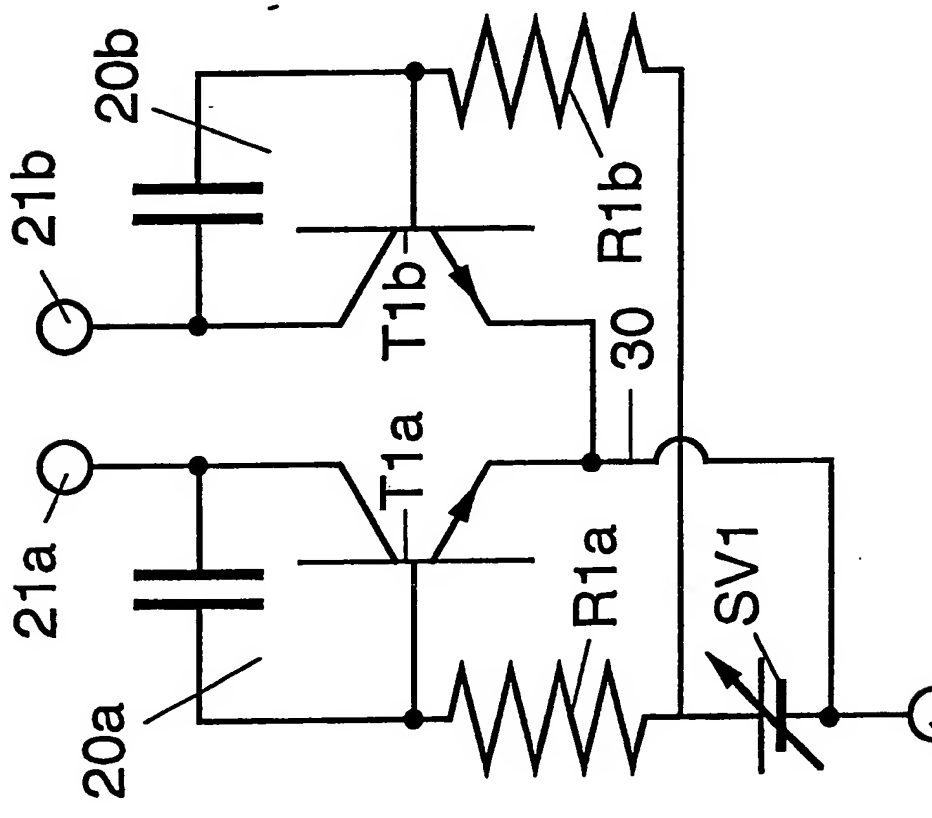
20b
21b
T1b
R1b
30
21a
T1a
20a
R1a
SV1
22

Fig. 3A.

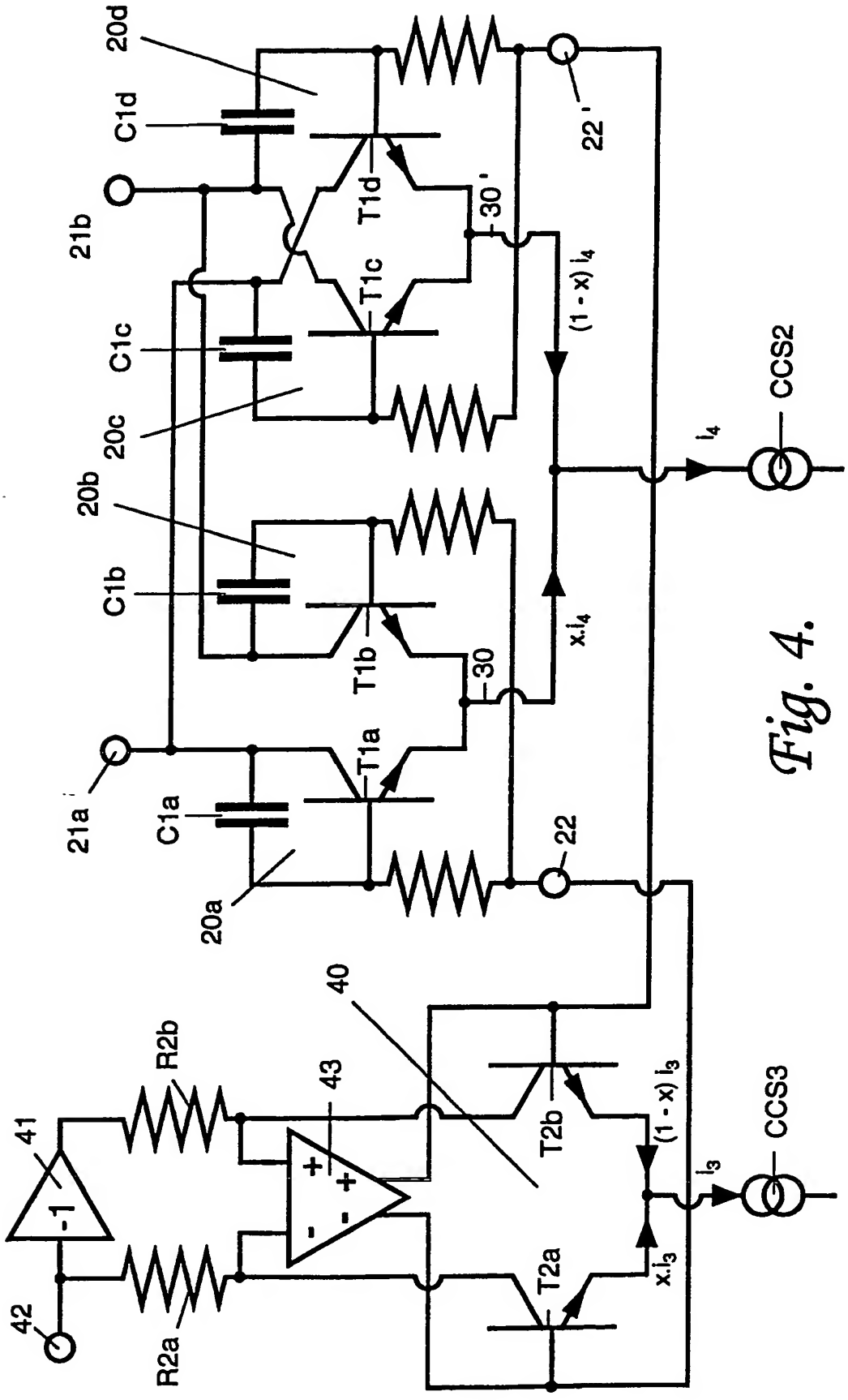
20d
C1d
T1d
30'
22'
21b
T1c
C1c
20c
(1 - x) I_4
20b
C1b
T1b
30
x.I_4
I_4
CCS2
21a
C1a
T1a
22
20a
40
R2b
43
T2b
(1 - x) I_3
41
-1
I_3
CCS3
T2a
x.I_3
42
R2a

Fig. 4.

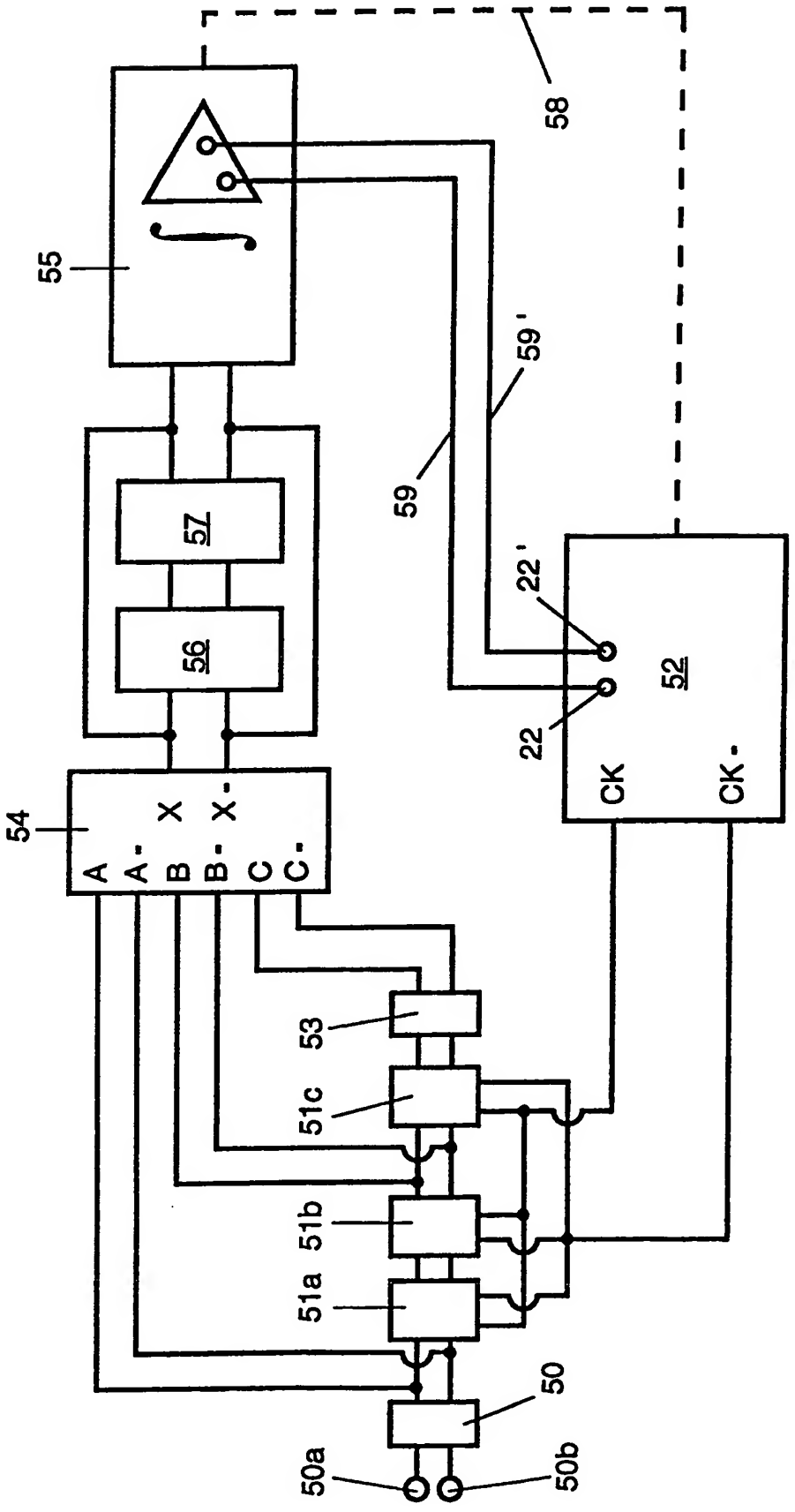
58
55
59'
59
57
56
22'
22
52
CK
CK-
54
A
A-
X
B
B-
X-
C
C-
53
51c
51b
51a
50
50a
50b

Fig. 5.

Voltage Controlled Oscillator

This invention relates to voltage controlled oscillators (VCO's). A well known form of VCO is the type of oscillator that uses a voltage controlled variable capacitance diode in the resonant circuit of the oscillator. Varying the voltage developed across such a diode varies its capacitance, and hence varies the resonant frequency of the resonant circuit. The capacitance of such a diode does not vary linearly with voltage, and hence the frequency of oscillation of a VCO regulated in this manner by such a diode varies non-linearly with voltage applied to that diode. Such non-linearity can be a problem, for instance if the VCO is being employed in a feedback loop for which critical damping is a requirement.

The present invention is directed to the provision of a VCO with a substantially linear voltage/frequency characteristic.

According to the present invention there is provided a voltage controlled oscillator having a resonant circuit possessing capacitance and inductance wherein at least a part of the capacitance of the resonant circuit is provided at an active port by an amplifier/fixed capacitor combination which presents an effective capacitance at the active port that is substantially linearly dependent upon the mutual conductance of the amplifier which mutual conductance is substantially linearly dependent upon the magnitude of an electrical signal applied to a control port of the amplifier.

A particular application for this type of VCO is in the construction of a digital clock extraction and data recovery circuit for use in a data transmission system.

There follows a description of VCO's embodying the invention in preferred forms, and of a digital clock extraction and data recovery circuit incorporating such a VCO. The description refers to the accompanying drawings in which:-

Figure 1 is a circuit diagram of a frequency controlled oscillator,

Figure 2 is a circuit diagram of a network for incorporation into the frequency controlled oscillator of Figure 1 in place of its variable capacitor in order to convert the structure into a voltage controlled oscillator (VCO),

Figures 3a, 3b and 4 depict alternative networks for use in place of the network of Figure 2, and

Figure 5 is a block diagram of a digital clock extraction and data recovery circuit incorporating a VCO employing the network of Figure 4.

Figure 1 depicts the basic components of a frequency tuneable oscillator comprising an amplifier 10 connected with a parallel resonant circuit comprising an inductor L and a variable capacitor C. Optionally a fixed capacitor C' may be connected in parallel with the variable capacitor C. The variable capacitor is depicted as being connected between a pair of terminals 11 which can be considered as forming an active port of the oscillator since it is the variation in the capacitance of the component that is connected across these terminals that effects the tuning of the oscillator. In the case of a voltage controlled oscillator the place of the variable capacitor C is taken by some device or structure, such as a variable capacitance diode, the magnitude of whose capacitance is electrically controllable. In the case of a variable capacitance diode, the potential difference developed across that diode determines the magnitude of its capacitance, but the relationship between the

potential difference and the capacitance is significantly non-linear, which can be a disadvantage in respect of its use in voltage controlled oscillators designed for certain applications. An alternative structure for connecting across terminals 11, one which possesses a substantially linear relationship between applied voltage and capacitance is depicted in Figure 2.

The circuitry of Figure 2 comprises a network, indicated generally at 20, that includes a transistor T1 with its collector and emitter respectively connected to terminals 21 and 22. A (fixed) capacitor C1 is connected between collector and base of the transistor T1 and the series combination of a resistor R1 and a low impedance adjustable voltage source VS1 is connected between its base and emitter. If the potential V of terminal 21 is increased so as to promote a current flow i_1 into capacitor C1 and an incremental current flow i_2 into the collector of transistor T1, then

$i_1 \approx C.\ dV/dt$ (provided R is small compared with $1/j\omega C$)

and $i_2 = g_m .i_1R = g_m .i_1R = g_m .R.C.dV/dt$

where g_m is the mutual conductance of T1. Therefore the total extra current flowing into terminal 20 as the result of the voltage increment is

$(i_1 + i_2) = (1 + g_mR)C.dV/dt$

and accordingly the capacitance presented by the circuitry of Figure 2 between terminals 21 and 22 is $C(1 + g_mR)$. Accordingly it is seen that this capacitance varies substantially linearly with g_m , which in its turn varies substantially with the value of the potential difference developed by the variable voltage source VS1.

In the single network 20 of Figure 2 the r.f. current flows through terminal 22, which is typically a ground terminal. This may be avoided by employing a balanced pair of such networks, 20a and 20b, operating in push-pull as depicted in Figure 3a. In this instance it is the terminals 21a and 21b that are connected across terminals 11 of Figure 1. It may be noted that, since the two networks are intended to function as a balanced pair operating in push-pull, the

d.c. component of the emitter currents of the two transistors T1a and T1b are matched, and hence it is sensible to employ a single adjustable voltage source VS1 common to both networks rather than to have a separate one for each of the two networks. The balanced push-pull arrangement ensure that there is no r.f. component of current flow in the tail connection 30 to the commoned emitters of T1a.and T1b, and accordingly an adjustable current source CCS1 can be employed, as depicted in Figure 3b, instead of the adjustable voltage source, as employed in the circuitry of Figure 3a. This entails connecting the resistors R1a and R1b direct to terminal 22 , disconnecting the tail connection 30 from terminal 22, connecting it instead to the adjustable constant current source CCS1.

The circuitry of Figure 3B is designed for regulating the value of the capacitance appearing between terminals 21a and 21b. This capacitance is shown to be a substantially linear function of the mutual conductance, g_m, of the two transistors T1a and T1b, which in its turn is a substantially linear function of collector current. Accordingly in this circuitry of Figure 3B the capacitance is regulated by control of the collector currents in the two transistors by the use of the adjustable constant current source CCS1 in the tail connection 30. Mutual capacitance, g_m, is also inversely proportional to absolute temperature and hence, in order to make the value of the capacitance appearing between terminals 21a and 21b independent of temperature, the constant current source is constructed in a form which makes the value of the current that it delivers directly proportional to absolute temperature.

Attention is now directed to the circuitry of Figure 4. This has two networks 20a and 20b in balanced push-pull arrangement corresponding to the networks 20a and 20b of Figure 3b, but with the sole difference that, in place of the adjustable constant current source CCS1 of Figure 3b, there is now a constant current source CCS2 which does not need to be adjustable though, like the constant current source CCS1, it does need to be constructed in a

form which makes the value of the current that it delivers directly proportional to absolute temperature. Additionally the circuitry of Figure 4 has a second pair of networks 20c and 20d, also in balanced push pull arrangement, that differ in only one respect from the networks 20a and 20b. This difference is that, whereas in networks 20a and 20b the capacitors C1a and C1b are connected between the bases and collectors of their own respective transistors T1a and T1b; in networks 20c and 20d the corresponding capacitors C1c and C1d are cross-connected between the base of one of the two corresponding transistors (T1c and T1d) and the collector of the other. The result of this cross-connection is that whereas in the case of networks 20a and 20b, the value of the mutual conductance, g_m, as determined by the current in the tail connection 30, produces positive capacitance across terminals 21a and 21b; in the case of networks 20c and 20d, the value of the mutual conductance, g_m, as determined by the current in the corresponding tail connection 30', produces negative capacitance across terminals 21a and 21b.

If each of the two pairs of networks 20a, 20b, and 20c, 20d were provided with its own constant current supply in its associated tail connection 30 or 30' then, by adjusting the relative magnitudes of the currents provided by those current sources, the mutual conductances of the four networks can be varied to take their contribution to the capacitance presented between terminals 21a and 21b from a positive value through zero to a negative value. In the particular circuit of Figure 4, only one constant current source, CCS2, is employed, and instead the current flow provided by that source is shared between the network pairs 20a, 20b and 20c, 20d in the ratio x : (1-x), where x lies between 0 and 1, its value being determined by the relation between the bias applied to terminal 22 and that applied to terminal 22'. These biases are in their turn determined by a network indicated generally at 40. This network comprises a pair of transistors T2a, T2b connected by their collectors, respectively via a resistor R2a, and via an inverter 41 and a matching resistor R2b, to a signal voltage input terminal 42. The

emitters of these two transistors are commoned and connected to a temperature independent constant current source CCS3. The bases of the two transistors T2a and T2b are respectively connected to the terminals 22 and 22'. A differential operational amplifier 43 connected between the collectors and bases of the two transistors T2a and T2b improves the linearity of the relationship between the magnitude of voltage applied to input terminal 42 and the ratio of the collector currents in the two transistors T2a and T2b.

The pair of transistors T2a and T2b form a 'master' pair of transistors in which the collector current ratio is constrained to be in a specific desired proportion. The connections between the bases of these two transistors are those of the four transistors T1a to T1d make the latter 'slave' transistors, so that the ratio of the currents in the tail connections 30 and 30' are constrained to be in the same specific desired proportion.

A particular application for the VCO described with particular reference to Figures 1 and 4 is in the construction of a digital clock extraction and data recovery circuit for use in a data transmission system, for instance one operating at about 620 Mbit/s. In such a circuit the output of a VCO is maintained by means of a critically damped phase locked loop (PLL) in a required phase relationship with respect to an extracted clock signal extracted from the data stream.

An example of such a digital clock extraction and data recovery circuit is schematically depicted in Figure 5. This circuit, except for its VCO and the control input thereto, is the same circuit as that specifically described in GB 2 251 142A (to which attention is directed). This circuit comprises an input (unclocked) buffer 50 to which the incoming data stream and its inverse are respectively applied on ports 50a and 50b, a cascade of three latches 51a, 51b an d 51c all clocked by a VCO 52 constituting a local clock, second (unclocked) buffer 53, a coincidence detector 54, an integrator 55

included in a phase locked loop (PLL) for phase adjustment of the VCO 52. Also included in the circuit is a frequency acquisition loop that includes the integrator 55, a lock slip detector 55 that provides a signal output in proportion to the frequency of the input thereto, and a charge pump 57 which causes the VCO 52 to sweep frequency when unlocked, but which has no effect in the phase-locked situation. Critical damping of the phase locked loop is achieved by appropriate choice of components values in the integrator 55.

The VCO 52 provides two local clock output signals CK and CK- that are the inverse of each other. These are applied to the three latches 51 to create, in conjunction with the buffers 50 and 53, six inputs A, A-, B, B-, C and C- to the coincidence detector 54. Where A identifies the output of the input buffer 50, B identifies the output of the second latch 51b and C identifies the output of the second buffer 53. The coincidence detector 54 is constructed to produce outputs X and X- in accordance with the general algorithm X=B. (A-C). Phase detection of the VCO output with respect to the input data is provided by comparison of the time lag between data transistors and clock edges of a certain direction. The two outputs X and X- of the coincidence detector 54 are differenced in a differential amplifier of the integrator 55 to provide an error voltage which is zero when the clock negative transistors are in synchronisation with the negative transistors of the incoming data.

In the circuit of GB 2 251 142A, the output of the integrator 54 is fed direct to the control input of the VCO 52 such a direct connection being represented in Figure 5 by the broken line 58. The same direct connection can also be employed in the present instance using the VCO of Figures 1 and 4, in which case the connection would be made to terminal 42 of Figure 4. Typically however the integrator 54 of Figure 5 may be constructed to include an operational amplifier having within it a pair of transistors in its signal path which may serve the function of T2a and T2b corresponding to the operational amplifier 43 of Figure 4, in which case unnecessary

component duplication can be avoided by dispensing with connection 58, and instead taking connections from this operational amplifier of the integrator 54 direct to terminals 22 and 22' of Figure 4 as depicted in Figure 5 by connections 59 and 59'.

CLAIMS:

1. A voltage controlled oscillator having a resonant circuit possessing capacitance and inductance wherein at least a part of the capacitance of the resonant circuit is provided at an active port by an amplifier/fixed capacitor combination which presents an effective capacitance at the active port that is substantially linearly dependent upon the mutual conductance of the amplifier which mutual conductance is substantially linearly dependent upon the magnitude of an electrical signal applied to a control port of the amplifier.

2. A voltage controlled oscillator as claimed in claim 1 wherein the amplifier/fixed capacitor combination includes first and second portions that are connected across the active port in mirror configuration to operate in balanced push-pull.

3. A voltage controlled oscillator as claimed in claim 2 wherein the amplifier/fixed capacitor combination additionally includes third and fourth portions connected across the active port in mirror configuration to operate in balanced push-pull, the amplifier being configured such that the electric signal applied to its control port determines the ratio of the sum of the current flows through the first and second portions to the sum of the current flows through the third and fourth portions, which first to fourth portions exhibit mutual conductances substantially linearly dependent upon the respective current flows therethrough, and wherein the first to fourth portions are respectively configured such that the current flows through the first and second portions contribute positively to the magnitude of the effective capacitance at the active port while the current flows through the third and fourth portions contribute negatively to the magnitude of the effective capacitance at the active port.

4. A voltage controlled oscillator substantially as hereinbefore described with reference to Figure 1 and Figures 2, 3a, 3b or 4 of the accompanying drawings.

5. A digital clock extraction and data recovery circuit incorporating a voltage controlled oscillator as claimed in any preceding claim.

6. A digital clock extraction and data recovery circuit which circuit incorporates a voltage controlled oscillator as claimed in claim 1, and is substantially as hereinbefore described with reference to Figure 5 of the accompanying drawings.